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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/823,276	03/29/2001	Ryo Inoue	10559-393001/P10258-ADI-	7293

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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 06/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/823,276	INOUE ET AL.	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *18 April 2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-21 have been considered.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as received on 18 April 2005 and IDS as received on 18 April 2005.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-21 are rejected under 35 U.S.C. 102(b) as being taught by Witt et al., U.S. Patent Number 6,018,798 (herein referred to as Witt).

5. Referring to claim 1, Witt has taught a method comprising in a processor which has a future file (Witt column 12, line 44; column 12, line 66 to column 13, line 7; and Figure 3) and which is capable of restoring the future file in a single clock cycle (Witt column 13, lines 40-46 and column 18, lines 54-67), restoring the future file over more than one clock cycle when a termination occurs in the processor (Witt column 19, lines 20-49).

6. Referring to claim 2, Witt has taught wherein the processor is a pipelined processor (Witt column 1, lines 15-20; column 5, lines 47-52; column 13, lines 23-27; column 22, lines 1-3; Figure 1; Figure 3; and Figure 13).

7. Referring to claim 3, Witt has taught wherein restoring the future file comprises updating at least some speculative registers in the future file with architectural values (Witt column 13, lines 23-33).

8. Referring to claim 4, Witt has taught wherein more than one clock cycle comprises two clock cycles (Witt column 19, lines 20-49).

9. Referring to claim 5, Witt has taught wherein more than one clock cycle comprises three clock cycles (Witt column 19, lines 20-49).

10. Referring to claim 6, Witt has taught wherein the processor is a pipelined processor (Witt column 1, lines 15-20; column 5, lines 47-52; column 13, lines 23-27; column 22, lines 1-3; Figure 1; Figure 3; and Figure 13) and more than one clock cycle comprises a number of clock cycles required to flush the processor (Witt column 13, lines 40-46 and column 19, lines 20-49).

11. Referring to claim 7, Witt has taught an apparatus comprising

a. A control unit coupled to a first set of registers, a second set of registers and a pipeline (Witt column 12, lines 45-65 and Figure 3),

b. The control unit adapted to restore the first set of registers with data contained in the second set of registers over more than one clock cycle following a termination of an instruction in the pipeline (Witt column 13, lines 40-46 and column 19, lines 20-49) although the control unit has the capability of restoring the first set of registers with data contained in the second set of registers in one clock cycle (Witt column 18, lines 54-67).

12. Referring to claim 8, Witt has taught wherein each register in the second set of registers is associated respectively with a register in the first set of registers (Witt column 12, line 66 to column 13, line 7).

13. Referring to claim 15, Witt has taught a system comprising:

a. A static random access memory device (Witt column 5, lines 53-55 and Figure 1). In regards to Witt, the static random access memory (SRAM) device is inherent to the instruction cache. Cache memory, like the instruction cache in Witt, are SRAMs (InstantWeb "static random access memory" ©1995)

b. A processor coupled to the static random access memory device (Witt column 5, lines 53-55 and Figure 1),

c. Wherein the processor includes a first set of registers, a second set of registers and a pipeline (Witt column 12, lines 45-65 and Figure 3),

d. A control unit adapted to restore the first set of registers with data contained in the second set of registers over more than one clock cycle following a termination of an instruction in the pipeline (Witt column 13, lines 40-46 and column 19, lines 20-49) although the control unit has the capability of restoring the first set of registers with data contained in the second set of registers in one clock cycle (Witt column 18, lines 54-67).

14. Referring to claims 9 and 16, Witt has taught wherein more than one clock cycle comprises two clock cycles (Witt column 19, lines 20-49).

15. Referring to claims 10 and 17, Witt has taught wherein more than one clock cycle comprises three clock cycles (Witt column 19, lines 20-49).

16. Referring to claims 11 and 18, Witt has taught wherein the control unit is further adapted to flush the pipeline following the termination of the instruction in the pipeline (Witt column 13, lines 40-46 and column 19, lines 20-49).

17. Referring to claims 12 and 19, Witt has taught wherein more than one clock cycle comprises the number of clock cycles required by the processor to flush the pipeline (Witt column 13, lines 40-46 and column 19, lines 20-49).

18. Referring to claims 13 and 20, Witt has taught the control unit further adapted to restore at least one register in the first set of registers after the pipeline has been flushed (Witt column 13, lines 40-46 and column 19, lines 20-49).

19. Referring to claims 14 and 21, Witt has taught wherein the pipeline is an X-stage pipeline (Witt column 1, lines 15-20; column 5, lines 47-52; column 13, lines 23-27; column 22, lines 1-3; Figure 1; Figure 3; and Figure 13), the control unit adapted to restore the first set of registers with data contained in the second set of registers over X-N clock cycles or fewer, following a termination of an instruction in an Nth stage of the pipeline (Witt column 19, lines 20-49 and column 22, lines 56-67).

Response to Arguments

20. Applicant's arguments filed 18 April 2005 have been fully considered but they are not persuasive. Applicant argues in essence on pages 6-7

> Witt column 19, lines 20-49 says nothing about how many clock cycles are used for restoration of the future file. If the future file described in column 18 is restored in a single clock cycle, as alleged by the Examiner, it would be reasonable to assume that it is also restored in a single clock cycle when explained

in more detail in column 19. Witt does not indicate at any point how many clock cycles are in fact used or that the number of clock cycles used is different than the number in which the processor is capable of restoring the future file.

21. This has not been found persuasive. To restore a future file, values are loaded into the future file from the physical registers that are known to be correct. Witt discloses in column 19, lines 40-49 that, even after a misprediction or exception, the pipeline continues executing with the current speculative values, thereby updating all registers in the future file affected by instructions, and only rebuilding data for the registers used by instructions dependent on the incorrect data. This means that all data stored in the future file that was not dependent on the incorrect data is kept, i.e. the correct data from the physical register that has already been stored in the corresponding future file is kept in the corresponding future file register. The registers that have data dependent on the incorrect data need to be rebuilt with the correct data. This means they need to now write the correct data from the corresponding physical registers in a cycle after the correct data was stored in the physical registers, which is after the other future file registers not dependent on the incorrect data have stored correct data from the physical registers.

Conclusion

22. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

23. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

25. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

26. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
24 June 2005

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